What is claimed is:

1. A data processing device which performs pipeline control, the data processing device comprising:

a fetch circuit which fetches instruction codes of a plurality of instructions in instruction queues, the instructions including a given target instruction and a prefix instruction which precedes the target instruction and modifies a function of the target instruction;

a prefix instruction decoder circuit which performs decode processing only on a prefix instruction, the prefix instruction decoder circuit receiving the instruction codes of the instructions before decoding that are fetched in the instruction queues, judging whether or not each of the instruction codes is a given prefix instruction, and causing a target instruction modifying information register to store information necessary for decoding the target instruction modified by the prefix instruction when the judged instruction code is the given prefix instruction; and

a general-purpose decoder circuit which receives each of the instruction codes of the instructions fetched in the instruction queues other than the prefix instruction as a decode instruction, and decodes the decode instruction,

wherein, when the decode instruction is the target instruction, the decoder circuit decodes the target instruction modified by the prefix instruction based on target instruction modifying information stored in the target instruction modifying information register.

2. The data processing device as defined in claim 1,

wherein the given prefix instruction includes an immediate-data expansion prefix instruction for expanding immediate data necessary for execution of the target instruction, function of which is expanded by the prefix instruction,

wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store immediate-data expansion information necessary for expanding the immediate data during execution of the target instruction modified by the immediate-data expansion prefix instruction when the input instruction code is the immediate-data expansion prefix instruction, and

wherein the decoder circuit decodes the decode instruction so that the immediate data is expanded at the time of execution of the target instruction that has been modified by the immediate-data expansion prefix instruction based on the immediate-data expansion information stored in the target instruction modifying information register when the decode instruction is the target instruction of the immediate-data expansion prefix instruction.

3. The data processing device as defined in claim 1,

wherein the given prefix instruction includes a shift prefix instruction for shifting an execution result of the target instruction, function of which is expanded by the prefix instruction,

wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store shift information necessary for shifting the execution results of the target instruction modified by the shift prefix instruction when the input instruction code is the shift prefix instruction, and

wherein the decoder circuit decodes the decode instruction so that the execution result of the target instruction modified by the shift prefix instruction are shifted based on the shift information stored in the target instruction modifying information register for execution of the target instruction when the decode instruction is the target instruction of the shift prefix instruction.

4. The data processing device as defined in claim 1,

wherein the given prefix instruction includes a register expansion prefix instruction for expanding a register necessary for execution of the target instruction, function of which is expanded by the prefix instruction,

wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store register expansion information necessary for expanding the register during execution of the target instruction modified by the register expansion prefix instruction when the input instruction code is the register expansion prefix instruction, and

wherein the decoder circuit decodes the decode instruction so that the register is expanded at a time of execution of the target instruction that has been modified by the register expansion prefix instruction based on the register expansion information stored in the target instruction modifying information register when the decode instruction is the target instruction of the register expansion prefix instruction.

5. The data processing device as defined in claim 1,

wherein the given prefix instruction includes an execution control prefix instruction for controlling whether or not to execute the target instruction, function of which is expanded by the prefix instruction,

wherein the prefix instruction decoder circuit causes the target instruction modifying information register to store execution control information necessary for controlling whether or not to execute the target instruction modified by the execution control prefix instruction when the input instruction code is the execution control prefix instruction, and

wherein the decoder circuit decodes the decode instruction so that the target instruction modified by the execution control prefix instruction is executed by judging whether or not to execute the target instruction based on the execution control information stored in the target instruction modifying information register when the

decode instruction is the target instruction of the execution control prefix instruction.

6. The data processing device as defined in claim 1,

wherein the fetch circuit is connected with a bus having a width at least twice the width of the instruction code, and fetches the instructions in the instruction queues through the bus in one clock cycle.

7. The data processing device as defined in claim 1,

wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction, and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction.

8. The data processing device as defined in claim 2,

wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction, and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction.

9. The data processing device as defined in claim 3,

wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction, and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction.

10. The data processing device as defined in claim 4,

wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction, and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction.

11. The data processing device as defined in claim 5,

wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction, and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction.

12. The data processing device as defined in claim 6,

wherein the target instruction is located subsequent to the prefix instruction which modifies the target instruction, and

wherein the prefix instruction decoder circuit performs decode processing only on the prefix instruction for a second instruction subsequent to a first instruction during a period in which the decoder circuit decodes the first instruction.

13. Electronic equipment comprising:

the data processing device as defined in claim 1;

means which receives input information; and

means which outputs a result processed by the data processing device based on the input information.

14. Electronic equipment comprising:

the data processing device as defined in claim 2;

means which receives input information; and

means which outputs a result processed by the data processing device based on the input information.

15. Electronic equipment comprising:

the data processing device as defined in claim 3;

means which receives input information; and

means which outputs a result processed by the data processing device based on the input information.

16. Electronic equipment comprising:

the data processing device as defined in claim 4;

means which receives input information; and

means which outputs a result processed by the data processing device based on the input information.

17. Electronic equipment comprising:

the data processing device as defined in claim 5;

means which receives input information; and

means which outputs a result processed by the data processing device based on the input information.

18. Electronic equipment comprising:

the data processing device as defined in claim 6;

means which receives input information; and

means which outputs a result processed by the data processing device based on the input information.

19. Electronic equipment comprising:

the data processing device as defined in claim 7;

means which receives input information; and

means which outputs a result processed by the data processing device based on the input information.